

IN THE CLAIMS:

Please cancel claims 1-17 and 22-29 and add new claims 30-40, as shown in the listing of claims below.

Claims 1-17 (canceled)

18. (Original) A circuit for compensating for phase differences between a plurality of signals associated with a plurality of signal levels, comprising:

a rising edge phase comparator for comparing a rising edge of a first signal associated with a first signal level with a rising edge of a second signal associated with a second signal level, for generating a rising edge compensation signal indicative of a phase difference between the rising edge of the first signal and the rising edge of the second signal;

a falling edge phase comparator for comparing a falling edge of the first signal with a falling edge of the second signal, for generating a falling edge compensation signal indicative of a phase difference between the falling edge of the first signal and the falling edge of the second signal; and

an adjustable delay buffer coupled to the rising edge comparator and the falling edge comparator, for delaying the rising edge of the first signal in response to the rising edge compensation signal and for delaying the falling edge of the first signal in response to the falling edge compensation signal.

19. (Original) The circuit of claim 18 wherein the adjustable delay buffer comprises:

at least one buffer transistor for buffering the first signal;

at least one rising edge control transistor, responsive to the rising edge compensation signal, for adjusting current flow through the at least one buffer transistor for controlling delay of the rising edge of the first signal through the at least one buffer transistor; and

at least one falling edge control transistor, responsive to the falling edge compensation signal, for adjusting current flow through the at least one buffer transistor for controlling the delay of the falling edge of the first signal through the at least one buffer transistor.

20. (Original) The circuit of claim 19 wherein:

the rising edge phase comparator comprises a register for determining whether the rising edge of the first signal leads the rising edge of the second signal; and

the falling edge phase comparator comprises a register for determining whether the edge of the second signal leads the falling edge of the first signal.

21. (Original) The circuit of claim 20 further comprising a plurality of low pass filters for filtering the rising edge compensation signal and the falling edge compensation signal.

Claims 22-29 (Canceled)

30. (New) The system of claim 18 further comprising at least one power supply for providing a plurality of supply voltages associated with the plurality of signal levels.

31. (New) The system of claim 18 wherein the first signal and the second signal are derived from a common clock signal.

32. (New) A method of compensating for phase differences between a plurality of signals associated with a plurality of signal levels, comprising steps of:

(a) comparing a rising edge of a first signal associated with a first signal level with a rising edge of a second signal associated with a second signal level;

(b) generating a rising edge compensation signal indicative of a phase difference between the rising edge of the first signal and the rising edge of the second signal;

(c) comparing a falling edge of the first signal with a falling edge of the second signal;

(d) generating a falling edge compensation signal indicative of a phase difference between the falling edge of the first signal and the falling edge of the second signal;

(e) delaying the rising edge of the first signal in response to the rising edge compensation signal; and

(f) delaying the falling edge of the first signal in response to the falling edge compensation signal.

33. (New) The method of claim 32 further comprising a step (e) of:
(g) buffering the first signal with a buffer transistor.
34. (New) The method of claim 33 wherein delaying step (e) comprises adjusting current flow through the buffer transistor, thereby controlling delay of the rising edge of the first signal through the buffer transistor.
35. (New) The method of claim 34 wherein delaying step (f) comprises adjusting current flow through the buffer transistor, thereby controlling delay of the falling edge of the first signal through the buffer transistor.
36. (New) The method of claim 35 wherein generating step (b) comprises generating a rising edge compensation signal indicative of whether the rising edge of the first signal leads the rising edge of the second signal.
37. (New) The method of claim 36 wherein generating step (d) comprises generating a falling edge compensation signal indicative of whether the falling edge of the first signal leads the falling edge of the second signal.
38. (New) The method of claim 37 further comprising a step (h) of:
(h) filtering the rising edge compensation signal and the falling edge compensation signal with low-pass filters.
39. (New) The method of claim 32 further comprising a step (g) of:
(g) providing a plurality of supply voltages associated with the plurality of signal levels.
40. (New) The method of claim 32 wherein the first signal and the second signal are derived from a common clock signal.